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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,488	01/21/2004	Young-Ho Kim	8836-225 (IB12190-US)	4065
22150	7590	05/25/2005	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			TRAN, MAI HUONG C	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/761,488

Applicant(s)

KIM ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 4-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of Group I (claims 1-3) drawn to a semiconductor device is acknowledged. Accordingly, claims 4-14 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentability of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103 (a) as being unpatentable over
Background of the invention in view of Cappelletti et al. (US 6,576,950).

Regarding to claim 1, Background of the Invention discloses an electrically erasable programmable read only memory (EEPROM) cell, comprising an isolation layer formed at a semiconductor substrate 10 to define an active region; a source region 40, a buried N+ region 16 and a drain region 42 formed at the active region and spaced apart from each other; a cell depletion region 38 formed at the active region between the buried N+ region 16 and the drain region 42, the buried N+ region 16 being in contact with the cell depletion region 38; a first channel region between the source region 40 and the buried N+ region 16; a second channel region between the cell depletion region 38 and the drain region 42; a memory gate 34 formed over the first channel region and the buried N+ region 16; a selection gate 36 formed over the second channel region; and

a tunnel oxide layer 22 formed on the buried N⁺ region 16 (Specification, pages 1-4, and fig. 4).

Background of the Invention doesn't disclose the distances between the edges of the tunnel oxide layer and the buried N⁺ region are equidistant. However, Cappelletti teaches the distances between the edges of the tunnel oxide layer and the buried N⁺ region are equidistant (fig. 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the distances between the edges of the tunnel oxide layer and the buried N⁺ region are equidistant, as taught by Cappelletti in order to guarantee the functionality and reliability of the memory device, and secondly to keep unchanged as far as possible the performance of the advanced-logic device on the technological platform (col. 1, lines 21-25).

Regarding to claim 2, Background of the Invention discloses the EEPROM cell wherein the memory gate 34 comprises a floating gate 24a; an inter-gate dielectric layer 30a on the floating gate; and a control gate electrode 32a on the inter-gate dielectric layer (Specification, pages 1-4, and fig. 4).

Regarding to claim 3, Background of the Invention discloses the EEPROM cell wherein the selection gate 36 comprises a lower selection gate 24b; an inter-gate dielectric layer 30b on the lower selection gate; and an upper selection gate 32b on the

inter-gate dielectric layer, the upper selection gate being electrically connected to the lower selection gate (Specification, pages 1-4, and fig. 4).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mai-Huong Tran